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DELAY LOCK CIRCUIT HAVING SELF-CALIBRATING LOOP

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Field of Invention

5 The present invention relates generally to signal generating circuit, and more particularly, to delay lock circuits.

Background

Many semiconductors devices such as memory devices use delay lock
10 circuits to generate an internal signal based on an external signal.

Some delay lock circuits use a feedback signal to obtain a measurement during an initialization. The feedback signal is a delayed version of the external signal. The measurement allows the delay lock circuits to synchronize the internal signal with the external signal.

15 Variations in elements such as manufacturing process, voltage, and temperature (PVT) may affect the measurement during the initialization. For example, the PVT variations may cause the delay lock circuits to spend more time to obtain the measurement, thereby increasing the time for the delay lock circuits to put the internal and external in synchronization. In some cases, the PVT variations
20 may cause the delay lock circuits to fail to get the measurement during the initialization, leading to malfunction of the device.

Summary of the Invention

The present invention provides circuits and methods for generating an
25 internal signal based on an external signal in which the circuits are less sensitive to PVT variations.

One aspect includes a delay lock circuit having a measuring path for receiving a reference signal to sample a pulse to obtain a measured delay. The delay circuit also includes a forward path for delaying the reference signal based on the
30 measured delay to generate an internal signal. The delay lock further includes a

feedback path connected to the measuring path and the forward path. The feedback path has a calibrating unit for generating the pulse based on a plurality of feedback signals generated from the reference signal. The calibrating unit is configured to conditionally adjust a pulse width of the pulse to allow the measured delay to be
5 obtained during the initialization.

Another aspect includes a method of generating an internal signal. The method generates a pulse with a pulse width. The pulse is sampled with a reference signal in an initialization to obtain a measured delay. During the initialization, the method conditionally adjusts the pulse width. The method delays the reference
10 signal based on the measured delay to generate the internal signal.

Brief Description of the Drawings

FIG. 1 shows a delay lock circuit according to an embodiment of the invention.

15 FIG. 2 is an exemplary timing diagram for the delay lock circuit of FIG. 1.

FIG. 3A is an exemplary timing diagram for the delay lock circuit of FIG. 1 having an initial pulse with a narrow pulse width.

FIG. 3B is an exemplary timing diagram for the delay lock circuit of FIG. 1 having an initial pulse with a wide pulse width.

20 FIG. 4 shows a circuit diagram of a portion of a calibrating unit according to an embodiment of the invention.

FIG. 5 shows the timing relationship among the signals of the circuit diagram of FIG. 4.

FIG. 6 shows the timing relationship among the signals of a generator.

25 FIG. 7 shows a memory device according to an embodiment of the invention.

FIG. 8 shows a system according to an embodiment of the invention.

Detailed Description of the Embodiments

The following description and the drawings illustrate specific embodiments
30 of the invention sufficiently to enable those skilled in the art to practice the

invention. Other embodiments may incorporate structural, logical, electrical, process, and other changes. In the drawings, like numerals describe substantially similar components throughout the several views. Examples merely typify possible variations. Portions and features of some embodiments may be included in or
5 substituted for those of others. The scope of the invention encompasses the full ambit of the claims and all available equivalents.

Figure 1 shows a delay lock circuit according to an embodiment of the invention. Delay lock circuit 100 receives an external clock signal XCLK and generates an internal clock signal DLLCLK. The XCLK signal propagates through
10 an input buffer 104 and becomes a reference signal CLKREF. Thus, the CLKREF signal is a version of the XCLK signal delayed by a time delay equal to the time delay of input buffer 104.

The CLKREF signal propagates through several signal paths including a measuring path 103, a forward path 105, and a feedback path 107.

15 Feedback path 107 includes a calibrating unit 110 for generating a calibrating signal CLKP based on feedback timing information of the CLKREF signal on feedback path 107. The CLKP signal includes one or more pulses as shown in FIG. 1. In some embodiments, the pulses of the CLKP signals have unequal pulse widths.

20 Measuring path 103 includes a measuring unit 120 for performing a measurement on the CLKP signal. A controller 140 obtains the result of the measurement. The result of the measurement represents a time delay, which is called a measured delay. Measuring unit 120 includes a chain of measuring delay elements 121. The measured delay is a time delay equal to the time delay of a
25 number of measuring delay elements 121. Thus, the measured delay corresponds to a number of measuring delay elements 121. Measuring path 103 further includes a monitoring unit 170 for monitoring the measurement performed by measuring unit 120.

Forward path 105 includes a main delay unit 130 for applying a delay (main
30 delay) to the CLKREF signal to generate the DLLCLK signal. The main delay is

based on the measured delay. Main delay unit includes a chain of main delay elements 133, which are similar to delay elements 121 of measuring unit 120. The main delay is a time delay equal to the time delay of a number of main delay elements 133 within main delay unit 130. Thus, the main delay corresponds to a number of main delay elements 133. The number of main delay elements 133 corresponding to the main delay is equal to the number of measuring delay elements 121 corresponding to the measured delay. Forward path 105 further includes a selector 150, a clock tree 160, and an output buffer 118.

Delay lock circuit 100 has an initialization process to obtain the measured delay to adjust the relationship between the XCLK and DLLCLK signals. In some embodiments, the XCLK and DLLCLK signals are not synchronized at the beginning of the initialization. Based on the measured delay measured by measuring unit 120, main delay unit 130 applies the main delay to the CLKREF signal to synchronize the XCLK and DLLCLK signals. Delay lock circuit 100 is locked (or in a locked position) after the measured delay is obtained and after main delay unit 130 applies the main delay (equal to the measured delay) to the CLKREF signal so that the XCLK and DLLCLK signals are synchronized.

Calibrating unit 110 of feedback path 107 includes a model delay segment 111, a selectable delay segment 112, and a generator 114. Model delay segment 111 delays a signal CLKREFD on feedback path 107 and provides a feedback signal CLKFB. Selectable delay segment 112 also delays the signal CLKREFD and provides a feedback signal CLKFBE. The CLKREFD signal is the CLKREF signal after the CLKREF signal propagates through selector 150 and clock tree 160. The CLKFBE and CLKFB signals are different delayed versions of the CLKREFD signal. The CLKFBE signal is the CLKREFD signal delayed by a first amount of delay. The CLKFB signal is the CLKREFD signal delayed by a second amount of delay unequal to the first amount of delay. Further, since the CLKREF signal is a delayed version of the XCLK signal and the CLKFBE and CLKFB signals are generated from the CLKREF signal, the CLKFBE and CLKFB signals are also delayed versions of the XCLK signal.

Clock tree 160 distributes signals to other components besides delay lock circuit 100. The signals distributed by clock tree 160 may be used as clock signal. For example, the DLLCLK signal is one of the signals distributed by clock tree 160.

Model delay segment 111 has a number of delay elements to delay a signal
5 by a time delay equal to the sum of the time delays caused by input buffer 104 and output buffer 118.

Selectable delay segment 112 has a number of delay elements. The difference in time delay between the CLKFB and CLKFBE signals is equal to the delay time of a portion of the number of the delay elements of selectable delay
10 segment 112.

Selector 150 may be a multiplexer having input nodes for receiving two signals including the DOUT signal and the CLKREF signal. The DOUT signal is a signal at an output node 131 of main delay unit 130. At the beginning of the initialization, selector 150 selects the CLKREF signal as the signal at an output node
15 151 of selector 150. After the measured delay is obtained, selector 150 selects the DOUT signal as the signal at output node 151.

Selector 150 is controlled by the states (signal levels) of a control signal CLTX. At the beginning of the initialization, the CLTX signal has a first state (e.g., low) to allow selector 150 to select the CLKREF signal to output node 151. After
20 the initialization, the CLTX signal has a second state (e.g., high) to allow selector 150 to select the DOUT signal to output node 151.

Monitoring unit 170 monitors a condition of the measuring unit 120 based on an end of line signal QEND and a propagation output signal CLKOUT. The QEND signal is activated (e.g., from low to high) when delay lock circuit 100 is not
25 locked after a measurement by measuring unit 120. The QEND signal is also activated when delay lock circuit 100 is locked after a measurement but a phase error exists between the CLKREF and CLKFB signals. The CLKOUT signal is activated to indicate that a pulse of the CLKP signal has propagated through the entire measuring unit 120. Monitoring unit 170 generates an adjust signal ADJ and
30 a reset signal RESET based on the QEND and CLKOUT signals. The RESET

signal resets measuring unit 120 to an initial state. The ADJ signal enables calibrating unit 110 to adjust the CLKP signal during the initialization. The ADJ signal represents one or more signals. In some embodiments, the ADJ signal represents one or more analog signals. In other embodiments, the ADJ signal
5 represents one or more digital signals. In FIG. 1, line 172 represents one or more lines to carry one or more analog signals or to carry one or more digital signals.

During the initialization, monitoring unit 170 monitors the condition of measuring unit 120 while the CLKP signal is sampled by measuring unit 120 using the CLKREF signal. Measuring unit 120 uses the CLKREF signal to mark the
10 number of measuring delay elements 121 that a pulse of the CLKP signal has propagated through. In some embodiments, measuring unit 120 includes latches. During the initialization, the CLKREF signal triggers a particular number of the latches to mark the number of measuring delay elements 121 that a pulse of the CLKP signal has propagated through. The number of measuring delay elements
15 121 that are marked corresponds to the measured delay. Controller 140 activates the CTLX signal when the measured delay is successfully obtained during the sampling. At main delay unit 130, the activated CLTX signal allows the CLKREF signal to enter the chain of main delay elements 133 at an entry point. From the entry point, the CLKREF signal propagates through a number main delay elements 133 to
20 become the DOUT signal. The activated CLTX signal also enables selector 150 to pass the DOUT signal to node 151 and subsequently to output buffer 118. At the output node of output buffer 118, the DOUT signal becomes the DLLCLK signal.

Monitoring unit 170 activates the ADJ signal during the initialization when the measured delay is not successfully obtained. When the ADJ signal is activated,
25 calibrating unit 110 adjusts the CLKP signal by generating a new pulse with a pulse width different than the pulse width used in the previous measurement. Depending on the condition of measuring unit 120 when the ADJ signal is activated, the pulse width of the new pulse for a new measurement is either smaller or greater than the pulse width of the previous pulse used in the previous measurement. Monitoring

unit 170 also activates the RESET signal to reset measuring unit 120 to an initial state. The measurement is repeated with the new pulse.

In some cases, the manufacturing process, voltage, and temperature variations may cause delay lock circuit 100 to unsuccessfully obtain the measured delay in an initial measurement. Modifying the pulse width of the pulse of the CLKP signal in subsequent measurements after the initial measurement allows the measured delay to be obtained during the initialization so that the DLLCLK signal can be eventually generated and synchronized with the XCLK signal.

FIG. 2 is an exemplary timing diagram for the delay lock circuit 100 of FIG. 1. Between times T0 and T2, the XCLK and DLLCLK signals are not synchronized. A delay D indicates a time delay needed to synchronize the XCLK and DLLCLK signals. The CLKP signal has an initial pulse 201 generated based on the CLKFB and CLKBE signals. A measured delay 211 is obtained after time T1. Measured delay 211 is a time delay corresponding to the delay D. After measured delay 211 is obtained, between time T1 and T2, controller 140 activates the CTLX signal. In response to the CTLX signal, main delay unit 110 applies a main delay 221 in main delay unit 130. The XCLK and the DLLCLK signals are synchronized at time T2 and delay lock circuit 100 is locked. After the CTLX signal is activated, the CLKFBE and CLKP signals are deactivated.

FIG. 2 shows three cycles of the XCLK signal between times T0 and T2 as an example. In some embodiments, more than three cycles of the XCLK signal may occur between times T0 and T2.

In the exemplary timing diagram of FIG. 2, the CTLX signal is activated to indicate that the measured delay is successfully obtained when pulse 201 is sampled. When the CTLX signal is activated, the QEND and RESET signals are not activated. Thus, the ADJ signal is also not activated. Therefore, no adjustment to the pulse width of pulse 201 is performed.

In some embodiments, delay lock circuit 100 is configured such that initial pulse 201 has an initial pulse width equal to a time delay of one delay element 121 or 133 of FIG. 1. Setting the initial pulse width equal to a time delay of one delay

element 121 or 133 reduces or eliminates the phase error between the XCLK and the DLLCLK signals when delay lock circuit 100 is locked. In FIG. 2, the initialization successfully synchronizes the XCLK and DLLCK signals and locks delay lock circuit 100 without modifying the pulse width of the initial pulse 201.

5 In some cases, the manufacturing process, voltage, and temperature variations may cause the pulse width of initial pulse 201 at time T0 to be either narrower or wider. Delay lock circuit 100 is configured to adjust the initial pulse having either the narrow pulse width or the wide pulse width. FIG. 3A and FIG. 3B below show exemplary timing diagrams for delay lock circuit 100 having an initial
10 pulse with a narrow pulse width and an initial pulse with a wide pulse width.

 FIG. 3A is an exemplary timing diagram for the delay lock circuit 100 of FIG. 1 having an initial pulse with a narrow pulse width. In FIG. 3A, the measured delay is unsuccessfully obtained between times T0 and T2 during a measurement of initial pulse 311. Thus, delay lock circuit 100 is not locked. A new pulse 312 is
15 generated with a pulse width greater than the pulse width of pulse 311. Thus, the pulse width of the pulse of the CLKP signal is adjusted.

 Between times T1 and T2, the QEND signal is activated indicating delay lock circuit 100 is not locked after the measurement between times T0 and T1. The CLKOUT signal is not activated between time T0 and T2 indicating that pulse 311
20 disappears inside measuring unit 120. A narrow pulse width may cause pulse 311 to disappear inside measuring unit. When the QEND signal is activated, the ADJ signal is activated to adjust the pulse width of pulse 311. Calibrating unit 110 (FIG. 1) adjusts the pulse width of pulse 311 by generating the new pulse 312 with a pulse width greater than the pulse width of pulse 311. The RESET signal is activated to
25 reset measuring unit 120 so that a new measurement can be performed on the new pulse 312. Between times T3 and T4, delay lock circuit 100 continues the initialization. A measured delay 321 is obtained based the measurement of pulse 312. The CTLX signal is activated. A main delay 322 is applied to allow the XCLK and DLLCLK to be synchronized at time T4. After the CTLX signal is
30 activated, the CLKFBE and CLKP signals are deactivated.

FIG. 3A shows five cycles of the XCLK signal between times T0 and T4 as an example. In some embodiments, more than five cycles of the XCLK signal may occur between times T0 and T4.

FIG. 3B is an exemplary timing diagram for the delay lock circuit 100 of FIG. 1 having an initial pulse with a wide pulse width. FIG. 3B describes a situation in which delay circuit 100 is locked with the entry point of the CLKREF signal into main delay unit 130 at one of the delay elements 133 (e.g., the first delay element) such that a phase error occurs between the CLKREF and CLKFB signals.

Delay lock circuit 100 is configured to reduce the time spent to correct the phase error by adjusting (e.g., reducing) the pulse width during the initialization. In FIG. 3B, a measured delay 360 is obtained between times T0 and T1 during a measurement of pulse 351. A phase error, indicated by PE, exists between the CLKREF and CLKFB signals because the entry point to measuring delay unit 120 and main delay unit 130 may be located at the first delay element 121 of measuring delay unit 120 and at the first delay element 133 of main delay unit 130. To correct the phase error, between times T1-T2, the ADJ signal is activated to adjust (e.g., reduce) the width of pulse 351. The RESET signal is also activated to reset measuring unit 120 to prepare for another measurement using a new pulse. The activated RESET signal also resets the state of the CTLX signal.

At time T2, a new pulse 352 is generated. Pulse 352 has a pulse width smaller than the pulse width of pulse 351. Between times T2 and T4, the process is similar to the process between times T0-T2 of FIG. 2. A new measured delay 361 is obtained based on the measurement of pulse 352. The CTLX signal is activated. A main delay 362 is applied to allow the XCLK and DLLCLK to be synchronized at time T4. After the CTLX signal is activated, the CLKFBE and CLKP signals are deactivated.

FIG. 3B shows five cycles of the XCLK signal between times T0 and T4 as an example. In some embodiments, more than five cycles of the XCLK signal may occur between times T0 and T4.

FIG. 4 shows a circuit diagram of a portion of calibrating unit 110 of FIG. 1. In FIG. 4, model delay segment 111 has an input node to receive the CLKREFD signal and an output node 401 to provide the CLKFB signal. Model delay segment 111 includes a delay chain 411 having a number of delay elements 451 (451-0 through 451-N) for delaying the CLKREFD signal. The CLKFB signal is the CLKREFD signal delayed by an amount of delay equal to the sum of the delays caused by all of the delay elements 451. In some embodiments, model delay segment 111 further includes elements similar to input buffer 104 and output buffer 118 (FIG. 1) for delaying the CLKREFD signal before the CLKREFD signal is provided to delay element 451-N.

Selectable delay segment 112 includes a delay chain 410 and a selector 420. Delay chain 410 has an input node to receive the CLKREFD signal, and a number of selectable output nodes to provide a number of selectable signals (or feedback signals) FBE1, FBE2, and FBE3. Selector 420 has a number of input nodes to receive the FBE1, FBE2, and FBE3 signals, and an output node 402 to provide the CLKFBE signal. The CLKFBE signal is the CLKREFD signal delayed by an amount of delay equal to a delay of a portion of the delay elements 412. In some embodiments, selectable delay segment 112 further includes elements similar to input buffer 104 and output buffer 118 (FIG. 1) for delaying the CLKREFD signal before the CLKREFD signal is provided to delay element 412-N.

Delay chain 410 includes a number of delay elements 412 (412-0, 412-1, 412-2, 412-3 through 412-N). Delay chain 410 has a subset 414. Subset 414 includes a number of delay elements 412-0, 412-1, and 412-2. Each of the delay elements within subset 414 provides one of the signals FBE1, FBE2, and FBE3. In FIG. 4, subset 414 includes three delay elements to provide three feedback signals (FBE1, FBE2, and FBE3) as an example. In some embodiments, the number of delay elements in subset 414 may be different from three to provide a different number of feedback signals. FIG. 5 shows the relationships among the FBE1, FBE2, and FBE3 signals, the CLKFB signal, and the CLKFBE signal.

In FIG. 4, selector 420 includes a number of switches 424, 425, and 426, and a storage 432. Each of the switches 424, 425, and 426 connects to an output node of a corresponding delay element of subset 414 to pass one of the FBE1, FBE2, and FBE3 signals to node 402 to become the CLKFBE signal. In some embodiments, switches 424, 425, and 426 include transistors having gates controlled by the values stored in storage 432.

Storage 432 includes a number of cells 434, 435, and 436, each storing a value. Examples of the value stored in each of the cells 434, 435, and 436 include logic one (high) and logic zero (low). The values in cells 434, 435, and 436 control the states of switches 424, 425, and 426. For example, if cell 434 has a logic one and both cells 435 and 436 have a logic zero, switch 424 is activated and switches 425 and 426 are not activated. In this example, switch 424 passes the FBE1 signal to node 402. The FBE1 signal becomes the CLKFBE signal at node 402. The value in each of the cells 434, 435, and 436 is changed after each time the ADJ signal is activated.

In some embodiments, cells 434, 435, and 436 form a shift register having an initial value to control switches 424, 425, and 426 such that each time the ADJ signal is activated, a different one of the FB1, FBE2, and FBE3 signals is selected to be the CLKFBE signal. For example, when the FBE2 signal is initially selected to be the CLKFBE signal, after the ADJ signal is activated, either the FBE3 signal or the FBE1 signal is selected to be the CLKFBE signal.

In some embodiments, line 172 includes multiple lines to carry multiple signals (e.g. two different signals) and the shift register formed by cells 434, 435, and 436 is shifted right or left to select the FB1, FBE2, and FBE3 signals based on the combination of the multiple signals. For example, when FBE2 is initially selected to be the CLKFBE signal, after the ADJ signal is activated, the FBE1 signal is selected to be the CLKFBE signal if the multiple signals on lines 172 have a first combination, e.g., the multiple signals on lines 172 have the same state. Using the same example, the FBE3 signal (instead of the FBE1 signal) is selected to be the

CLKFBE signal if the multiple signals have a second combination, e.g., the multiple signals on lines 172 have different states.

Monitoring unit 170 and controller 140 (FIG. 1) are configured to control the states of the multiple signals on lines 172. For example, controller 140 may include circuit elements to monitor the entry point of the CLKREF signal in measuring unit 120 and main delay unit 130. Based on the location of the entry point, controller 140 controls a state of one of the signals on multiple lines (172) such that cells 434, 453, and 436 enable switches 424, 425, and 426 to appropriately select the FBE1, FBE2, and FBE3 signals.

FIG. 5 shows the timing relationship among the signals of model delay segment 111 selectable delay segment 112 of FIG. 4. Label “d” represents a delay unit equal to a time delay of each of delay elements 412 (FIG. 4). Each of the FBE1, FBE2, and FBE3 signals has a rising edge occurred earlier than a rising of the CLKFB signal by a multiple of the unit delay “d”. For example, rising edge 501 of the FBE1 signal occurs one delay unit “d” earlier than rising edge 500 of the CLKFB signal. Rising edge 502 of the FBE2 signal occurs “2d” earlier than rising edge 500 of the CLKFB signal. Rising edge 503 of the FBE3 signal occurs “3d” earlier than rising edge 500 of the CLKFB signal. As described above in FIG. 4, depending on the states of switches 424, 425, and 426, the CLKFBE signal in FIG. 5 is one of the FBE1, FBE2, and FBE3 signals. FIG. 5 shows the CLKFBE signal being the FBE1 signal as an example.

FIG. 6 shows the timing relationship among the signals of generator 114 of FIG. 1. In FIG. 6, the CLKP1 and CLKP2 signals represent two exemplary cases for the CLKP signal of FIG. 1. Thus, the CLKP signal of FIG. 1 may be either the CLKP1 signal or the CLKP2 signal of FIG. 6.

The CLKP1 signal has a pulse 601 with a pulse width W1. The CLKP2 signal has a pulse 602 with a pulse width W2. W2 is greater than W1. Pulse 601 is generated from the CLKFB and the CLKFBE1 signals. Pulse 602 is generated from the CLKFB and the CLKFBE2 signals. The CLKFBE1 and CLKFBE2 signals correspond to the FBE1 and FBE2 signals of FIG. 4, respectively.

In FIG. 6, the CLKFBE1 signal has a rising edge occurred earlier than the rising edge of the CLKFB signal by one unit delay or one “d”. As shown in FIG. 6, the pulse width W1 of pulse 601 is equal to one delay unit. The pulse width W2 of pulse 602 is equal to two delay units.

5 In FIG. 6, the falling edge of each of the CLKP1 and CLKP2 signals aligns or corresponds with the rising edge of the CLKFB signal. Generating the CLKP1 or CLKP2 signal with the falling edge aligned with the rising edge of the CLKFB signal reduces a phase error between the CLKFB and CLKREF signals so that the XCLK and DLLCLK is more accurately synchronized.

10 Figure 7 shows memory device according to an embodiment of the invention. Memory device 700 includes a memory array 702 having plurality of memory cells arranged in rows and columns. The memory cells are grouped into a plurality of memory banks indicated by bank 0 through bank M (banks 0-M). Row decode 704 and column decode 706 access the memory cells in response to address
15 signals A0 through AX (A0-AX) on address lines (or address bus) 708. A data input path 714 and a data output path 716 transfer data between banks 0-M and data lines (or data bus) 710. Data lines 710 carry data signals DQ0 through DQN (DQ0-DQN). A memory controller 718 controls the modes of operations of memory device 700 based on control signals on control lines 720. The control signals
20 include, but are not limited to, a Chip Select signal CS*, a Row Access Strobe signal RAS*, a Column Access Strobe CAS* signal, a Write Enable signal WE*, and an external signal XCLK.

Memory device 700 further includes a delay lock circuit 705 for delaying the XCLK signal to generate an internal signal DLLCLK. The DLLCLK signal serves
25 as a clock signal to control a transfer of data on data output path 716. Delay lock circuit 705 includes embodiments of delay lock circuit 100 (FIG. 1). In some embodiments, the XCLK signal is provided to memory device from an external source externally to memory device 700.

Memory device 700 may be a dynamic random access memory (DRAM)
30 device. Examples of DRAM devices include synchronous DRAM commonly

referred to as SDRAM, SDRAM II, SGRAM (Synchronous Graphics Random Access Memory), DDR SDRAM (Double Data Rate SDRAM), DDR II SDRAM, DDR III SDRAM, GDDR III SDRAM (Graphic Double Data Rate), and Rambus DRAM devices. Memory device 700 includes other elements, which are not shown
5 for clarity.

FIG. 8 shows a system 800. System 800 includes a processor 810, a memory device 820, a memory controller 830, a graphic controller 840, and an input and output (I/O) controller 850, a display 852, a keyboard 854, a pointing device 856, and a peripheral device 858. A bus 860 couples all of these devices together.
10 A clock generator 870 provides a clock signal to at least one of the devices of system 800 via bus 860. An example of clock generator 870 includes an oscillator in a circuit board such as a motherboard. Two or more devices shown in system 800 may be formed in a single chip.

Memory device 820 includes memory device 700 (FIG. 7). Further, at least
15 one of the devices shown in system 800 includes delay lock circuit such as delay lock circuit 100 (FIG.1).

Bus 860 may be interconnect traces on a circuit board or may be one or more cables. Bus 860 may also couple the devices of system 800 by wireless means such as by electromagnetic radiations, for example, radio waves. Peripheral device 858
20 may be a printer, an optical device such as CD-ROM and DVD reader and writer, a magnetic device reader and writer such as a floppy disk driver, or an audio device such as a microphone.

System 800 represented by FIG. 8 includes computers (e.g., desktops, laptops, hand-helds, servers, Web appliances, routers, etc.), wireless communication
25 devices (e.g., cellular phones, cordless phones, pagers, personal digital assistants, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, camcorders, digital cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games, watches, etc.), and the like.
30

Conclusion

Various embodiments of the invention provide a delay lock circuit for generating an internal signal based on an external signal. The delay lock circuit includes a calibrating unit to conditionally adjust a pulse width of a pulse. During
5 an initialization process, the delay lock circuit performs a measurement on the pulse to put the internal and external signals in synchronization. Although specific embodiments are described herein, those skilled in the art recognize that other embodiments may be substituted for the specific embodiments shown to achieve the same purpose. This application covers any adaptations or variations of the present
10 invention. Therefore, the present invention is limited only by the claims and all available equivalents.